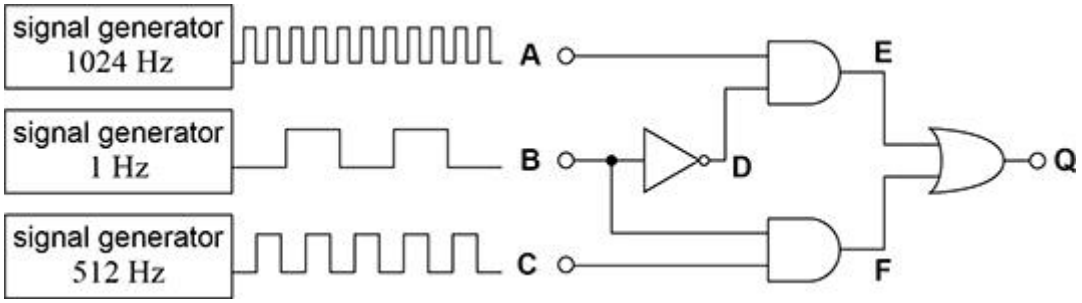
Q1.

A toy manufacturer is designing a two-tone siren for use in small battery-operated cars.
Figure 1 shows design Option **1**.

Option **1** uses three separate signal generators feeding into a logic sub-system. The signal generators produce logic-compatible 9 V square waves of frequencies 1024 Hz, 1 Hz and 512 Hz.

Figure 1



The waveforms shown are not to scale.

(a) Explain how the logic level applied at **B** in **Figure 1** determines the output frequency at **Q**.

_____

_____

_____

_____

_____

_____

(2)

(b) Write the Boolean algebra expression for output **Q** in terms of the inputs **A**, **B** and **C**.
Use only the logic operations shown in **Figure 1**.

Q = _____

(2)

(c) Option **1** is tested by replacing the 1 Hz signal generator with a manual input.

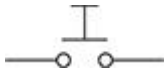
The manual input is provided by the combination of a push-to-make switch and a 10 kΩ resistor.

The combination produces the following voltages at its output:

- 0 V when the switch is not pressed
- 9 V when the switch is pressed.

Figure 2 shows the symbol for the push-to-make switch.

Figure 2



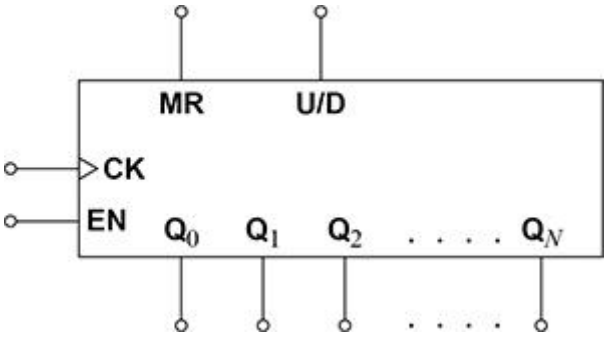
Complete **Figure 3** to show how this switch and the 10 kΩ resistor are connected. Label the output V_{out}.
You do not need to add details taken from **Figure 1**.

Figure 3

(1)

(d) **Figure 4** shows a generalised layout of an integrated circuit (IC) for an N-bit binary counter.
$\mathbf{Q}_0$ is the output that provides the least significant bit.

Figure 4



A signal generator feeds a square wave of frequency 1024 Hz into the clock of the IC. The N-bit binary counter generates the 512 Hz signal and the 1 Hz signal from separate outputs.

Deduce which of the outputs $\mathbf{Q}_0$ to $\mathbf{Q}_N$ will provide the 1 Hz signal.

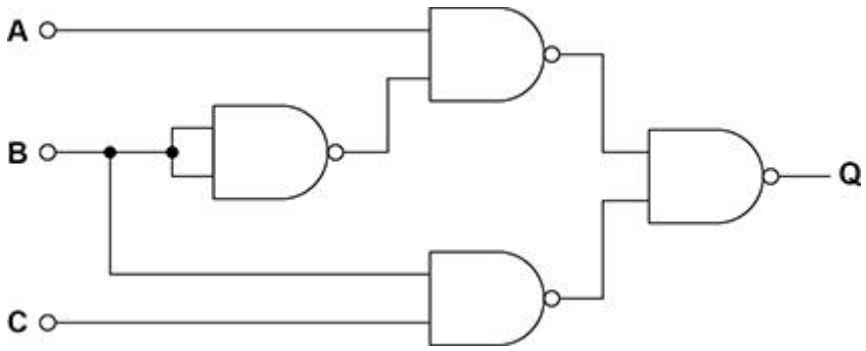
_____

(1)

(e) To make the two-tone siren, the manufacturer decides to use a new design, Option **2**.

Option **2** contains:
- one 1024 Hz signal generator
- one N-bit binary counter
- a new logic sub-system as shown in **Figure 5**.

Figure 5



Assume that:
- each **type** of logic gate has its own dedicated IC chip
- each separate signal generator is based upon its own IC chip.

Compare the number of ICs used in Option **1** with the number used in Option **2**.
Go on to explain **one** advantage of the manufacturer's decision.

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(2)

(Total 8 marks)

Q2.

The short message service (SMS) on a mobile phone can send a maximum of 160 characters per message. Each character is represented by its own seven-bit binary code as it is converted to digital data.

(a) The mobile phone transmits digital data at a rate of 8 kilobytes per second ($\mathrm{kB\ s^{-1}}$) when using the SMS function.

Determine the minimum time required to send 160 characters.

time = _____ s

(2)

Electrical noise can affect communication systems.

(b) Describe **one** origin of electrical noise in a communication system.

_____

_____

_____

(1)

(c) Describe the effect that electrical noise can have:

- on the signal and
- on the communication system.

_____

_____

_____

_____

_____

_____

_____

_____

(2)

Figure 1 shows a noisy digital signal V_{in} which is applied to a circuit.

The circuit output V_{out} switches to:

- 5 V when the input voltage V_{in} falls below 1.8 V
- 0 V when the input voltage V_{in} rises above 3.2 V.

Figure 1

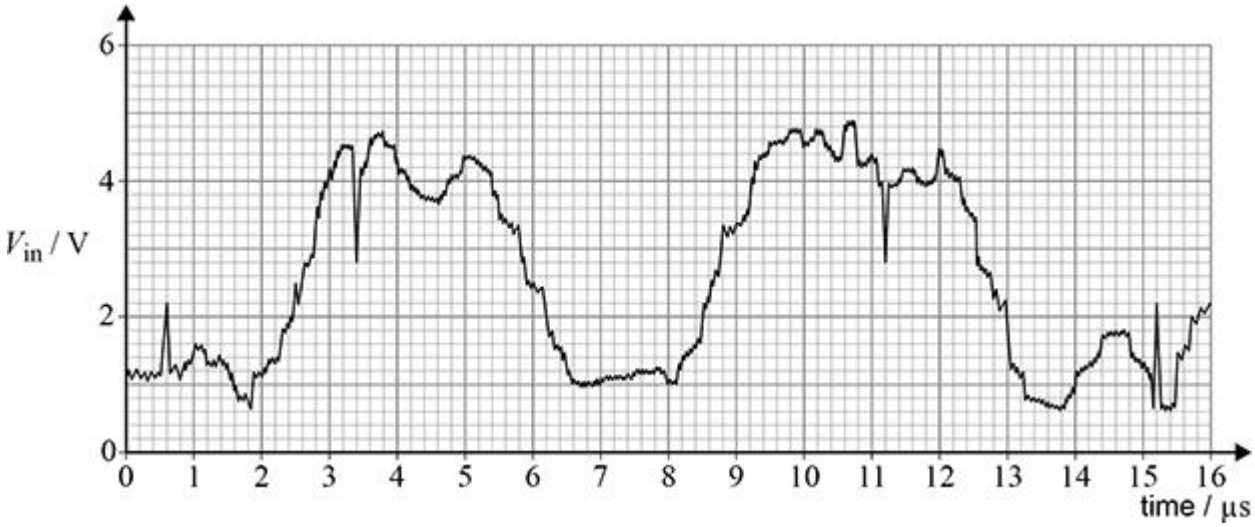
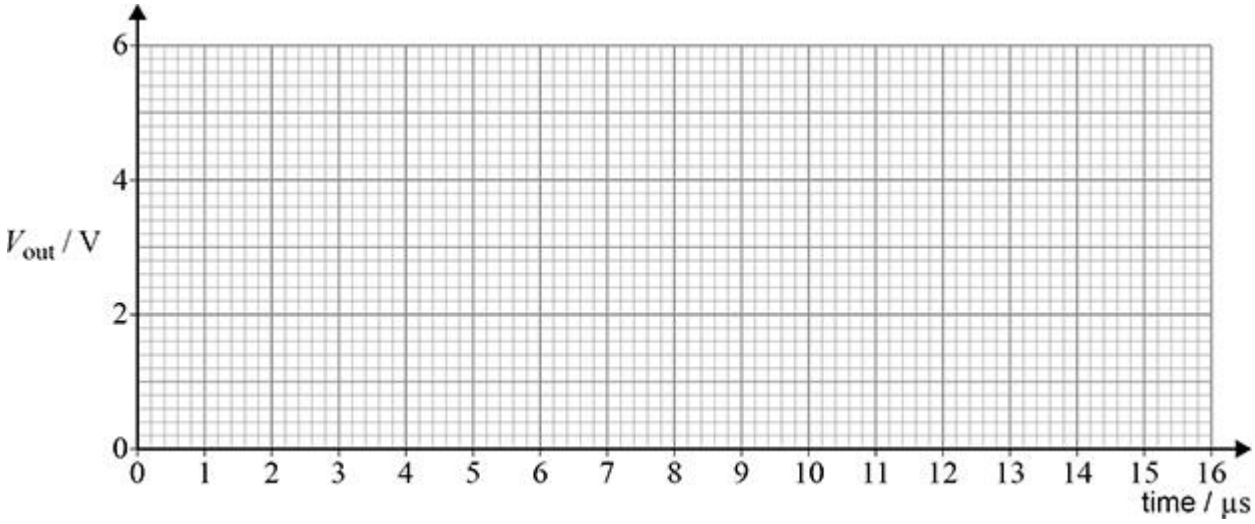


Figure 2



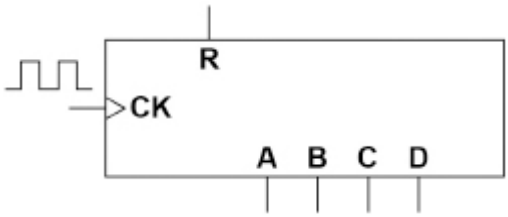
(d) Draw, on **Figure 2**, the output signal V_{out} from the circuit.
Assume that V_{out} is initially at 5 V.

(2)

(Total 7 marks)

Q3.

Figure 1 shows the input and output pins for a 4-bit binary counter. The output pin for the least significant bit is **A**.

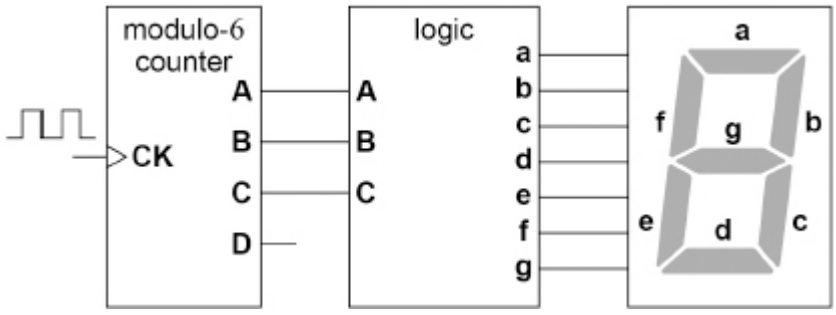


(a) Complete **Figure 1** by adding a single logic gate to the binary counter so that the circuit functions as a modulo-6 counter.

(2)

Figure 2 shows three outputs of the modulo-6 counter connected to a logic sub-system that controls a 7-segment display.
The decimal point on the display is not shown.
The whole system shown in **Figure 2** is to be used as an electronic dice.

Figure 2



Segments in the 7-segment display are turned on or off by the logic sub-system to display the decimal numbers 1 to 6 in sequence.
A segment in the display turns on when the logic output with the same letter as the segment is at logic 1.

The table below shows how the values of **CBA** control the logic level applied to each of the segments **a** to **g** during the counting cycle.

Logic inputs			**Logic outputs**						
C	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	1	1	0	0	0	0
0	0	1	1	1	0	1	1	0	1
0	1	0	1	1	1	1	0	0	1
0	1	1	0	1	1	0	0	1	1
1	0	0	1	0	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1

(b) One of the logic outputs **a** to **g** is controlled by a single NOT gate. This gate uses one of the inputs **A**, **B** or **C**.

State the input that is used and the segment that this NOT gate controls.

input = _____

segment = _____

(1)

(c) **X** represents one of the logic outputs. The Boolean expression for this output is:

$$\mathbf{X} = (\mathbf{A} \cdot \mathbf{B}) + \mathbf{C}$$

State which of the logic outputs **a** to **g** is being controlled by this function.

logic output = _____

(1)

(d) **Y** represents another of the logic outputs. The Boolean expression for this output is:

$$Y = \left(\overline{A} \cdot \overline{B}\right) + \left(\overline{\overline{B} \cdot \overline{C}}\right)$$

Complete **Figure 3** to show the combination of logic gates needed to represent the expression.
You should only use logic gates that represent the individual functions shown in the expression.

Figure 3

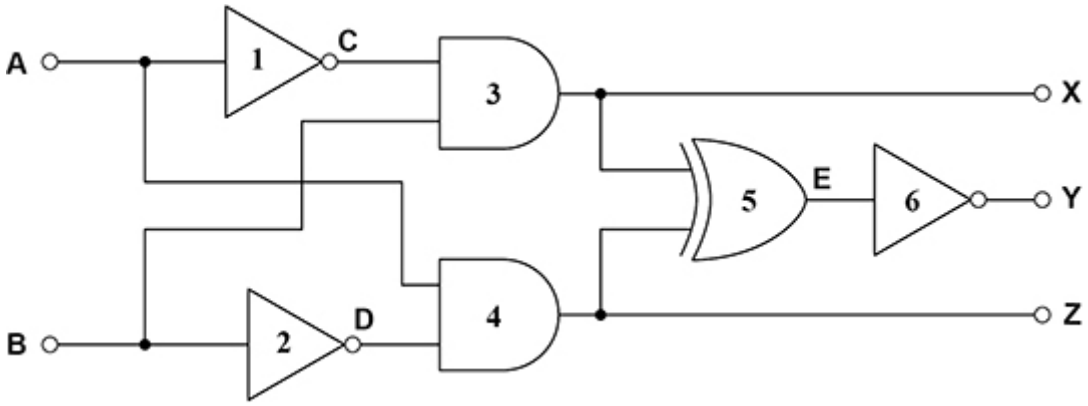
(3)

(Total 7 marks)

Q4.

The diagram below shows a logic system made of logic gates labelled **1** to **6**

The logic system has inputs **A** and **B** and outputs **X**, **Y** and **Z**.



(a) Write the simplest Boolean algebra expression for output **X** in terms of inputs **A** and **B**.

X = _____

(2)

(b) State the name of logic gate **5** in the figure above.

_____

(1)

(c) Complete the table below, the truth table for this logic system.

B	A	C	D	E	X	Y	Z
0	0	1	1	0			
0	1	0	1	1			
1	0	1	0	1			
1	1	0	0	0			

(2)

(d) Suggest a single logic gate that can replace the combination of gates **5** and **6** in this system.

_____

(1)

(e) The logic system in above diagram is designed to indicate which of inputs **A** and **B** has the larger binary value, or whether the values are the same. Each decision is indicated by one of the outputs **X**, **Y** or **Z** becoming a logic 1

Which row identifies the outputs **X**, **Y** and **Z**?

Tick (✓) **one** box.

X	Y	Z	
A = B	A < B	A > B	
A < B	A = B	A > B	
A < B	A > B	A = B	
A > B	A = B	A < B	

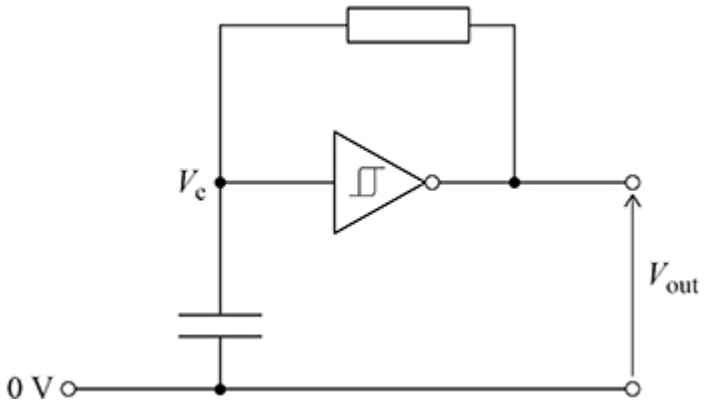
(1)

(Total 7 marks)

Q5.

Figure 1 shows a type of NOT gate called a Schmitt Trigger. This is connected to a capacitor of capacitance C and a resistor of resistance R to make an oscillator circuit. The circuit is used to produce continuous clock pulses.

Figure 1



V_{out} switches HIGH or LOW when the input voltage V_c passes through one of two trigger voltage values.

The output voltage V_{out} switches to:

- LOW when V_c rises and reaches the upper trigger voltage V_U
- HIGH when V_c falls and reaches the lower trigger voltage V_L.

(a) Initially the capacitor is uncharged and V_c is at $0\ \text{V}$.

Explain the sequence of actions of this circuit as the output goes through one full cycle. The first two stages have been done for you.

You should refer to the RC circuit in **Figure 1** and to V_U and V_L in your answer.

Stage 1: Since V_c is LOW, the output is HIGH.

Stage 2: The capacitor now charges through the resistor, making V_c rise.

Stage 3: _____

_____

_____

Stage 4: _____

_____

_____

Stage 5: _____

_____

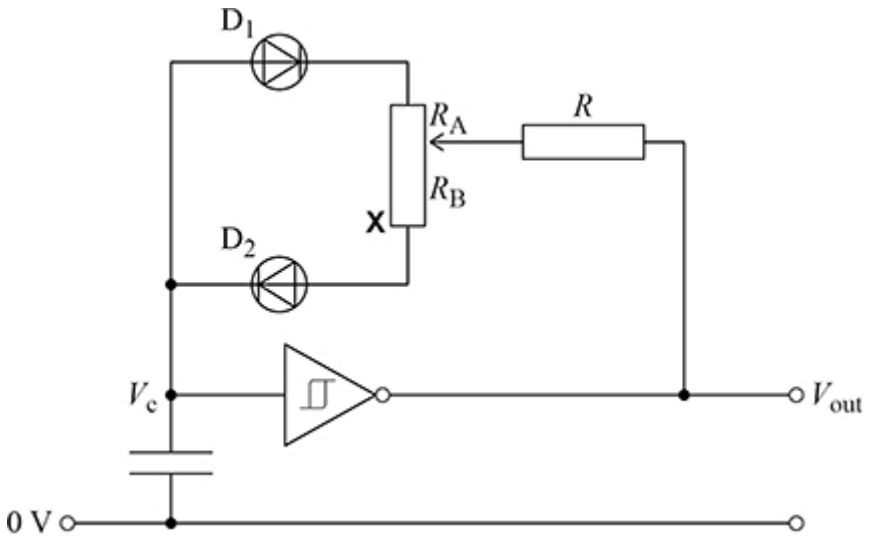
_____

(3)

(b) **Figure 2** shows the oscillator circuit after it has been modified by the addition of:

- two diodes D_1 and D_2
- a potential divider that has a total resistance value of (R_A + R_B).

Figure 2



In this particular circuit:

- the time t_H for the output signal to be HIGH is given by $t_H = 0.7C(R + R_B)$
- the time t_L for the output signal to be LOW is given by $t_L = 0.7C(R + R_A)$.

The slider of the potential divider is moved towards **X**, as shown in **Figure 2**.

State and explain the effect of this change on:

- the mark-to-space ratio (t_H : t_L)
- the pulse rate frequency (PRF).

mark-to-space ratio _____

_____

_____

_____

_____

_____

PRF _____

_

_____

_____

_____

_____

_____

(4)

(Total 7 marks)